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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,314	10/27/2000	David Carrel	4906.P012	6295

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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2668	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,314	CARREL, DAVID	
	Examiner	Art Unit	
	Clemence Han	2668	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-19 and 23-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-19 and 23-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 5-19 and 23-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al. (US Patent 6,850,531) in view of Ortega et al. (US 6,711,162).

Regarding claim 1 and 19, Rao teaches a method comprising: receiving a number of Internet Protocol (IP) packets on a real circuit and a number of virtual circuits, wherein the number of virtual circuits are within the real circuit such that the number of Internet Protocol (IP) packets on the real circuit have an IP over Ethernet encapsulation and the number of Internet Protocol (IP) packets on the number of virtual circuits have a Point-to-Point over Ethernet encapsulation (Column 24 Line 30-39); deencapsulating the number of Internet Protocol (IP) packets having the IP over Ethernet encapsulation (Column 6 Line 61-62); deencapsulating the number of Internet Protocol (IP) packets having the Point-to-Point over Ethernet encapsulation (Column 6 Line 61-62); and forwarding the

number of Internet Protocol (IP) packets having the IP over Ethernet encapsulation and the Point-to-Point over Ethernet encapsulation based on an address stored in the number of Internet Protocol (IP) packets (Column 12 Line 6-15). Rao, however, does not disclose concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets. Ortega teaches concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets (step 5A and 5B in Figure 7). It would have been obvious to one skilled in the art to modify Rao to receive IP over Ethernet packets and Point-to-Point over Ethernet packets concurrently as taught by Ortega in order to support various networking protocols (Column 7 Line 2-4).

Regarding claim 5 and 23, Rao teaches a method comprising: receiving a number of Internet Protocol (IP) packets over Ethernet on a real circuit, each IP packet over Ethernet having an Ethernet header and an IP address (Column 24 Line 30-39); removing the Ethernet header from the number of IP packets (Column 6 Line 61-62); receiving a number of IP packets within a Point-to-Point Protocol (PPP) over Ethernet on at least one virtual circuit, wherein each of the number of IP packets within the PPP over Ethernet includes a PPP header, a PPP over Ethernet (PPPoE) header, an Ethernet header and an IP address, wherein the at least one virtual circuit runs within the real circuit (Column 24 Line 30-39);

removing the PPP header and the PPPoE header from the number of IP packets within the PPP over Ethernet (Column 6 Line 61-62); removing the Ethernet header from the number of IP packets within the PPP over Ethernet (Column 6 Line 61-62); and forwarding the number of IP` packets over Ethernet and the number of IP packets within PPP over Ethernet based on the IP address (Column 12 Line 6-15). Rao, however, does not disclose concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets. Ortega teaches concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets (step 5A and 5B in Figure 7). It would have been obvious to one skilled in the art to modify Rao to receive IP over Ethernet packets and Point-to-Point over Ethernet packets concurrently as taught by Ortega in order to support various networking protocols (Column 7 Line 2-4).

Regarding claim 6, 11, 24 and 29, Rao teaches the number of IP packets over Ethernet and the number of IP packets within the PPP over Ethernet encapsulated in an Asynchronous Transfer Mode (ATM) protocol layer (Column 24 Line 30-39).

Regarding claim 7, 12, 25 and 30, Rao teaches removing the ATM protocol layer from the number of IP packets over Ethernet and the number of IP packets within the PPP over Ethernet (see Figure 28 and Column 6 Line 61-62).

Regarding claim 8, 13, 17, 26 and 31, Rao teaches calculating the number of IP packets within the PPP over Ethernet that are being received from the at least one virtual circuit (Column 22 Line 4-7).

Regarding claim 9, 14, 18, 27 and 32, Rao teaches performing rate limiting on the at least one virtual circuit based on the number of calculated IP packets within the PPP over Ethernet (Column 21 Line 53-56).

Regarding claim 10 and 28, Rao teaches a method comprising: receiving a number of different data packets over Ethernet on both a real circuit and a number of virtual circuits running within the real circuit (Column 24 Line 30-39); recursively performing the following for each of the number of different data packets: upon determining that a received data packet is an Internet Protocol (IP) packet over Ethernet on the real circuit (Column 11 Line 39-41), removing an Ethernet header from the received data packet (Column 6 Line 61-62) and forwarding the IP packet based on an IP address stored in the IP packet (Column 12 Line 6-15); and upon determining that a received data packet is an IP packet within a Point-to-Point Protocol (PPP) over Ethernet on one of the number of virtual circuits (Column 11 Line 39-41), removing an Ethernet header, a PPP header and a PPP over Ethernet (PPPoE) header from the data packet (Column 6 Line 61-62) and forwarding the IP packet based on an IP address stored in the IP

packet (Column 12 Line 6-15). Rao, however, does not disclose concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets. Ortega teaches concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets (step 5A and 5B in Figure 7). It would have been obvious to one skilled in the art to modify Rao to receive IP over Ethernet packets and Point-to-Point over Ethernet packets concurrently as taught by Ortega in order to support various networking protocols (Column 7 Line 2-4).

Regarding claim 15, Rao teaches a network element 10, 14 comprising: a number of input/output (I/O) cards (Figure 2) coupled to a number of real circuits, wherein each of the number of real circuits include at least one virtual circuit, the number of I/O cards to receive a number of Internet Protocol (IP) packets over Ethernet having an IP over Ethernet encapsulation on the real circuit, to receive a number of IP packets within a Point-to-Point Protocol (PPP) over Ethernet encapsulation on the at least one virtual circuit (Column 24 Line 30-39), to deencapsulate the number Internet Protocol (IP) packets having the IP over Ethernet encapsulation (Column 6 Line 61-62) and to deencapsulate the number of Internet Protocol (IP) packets having the Point-to-Point Protocol over Ethernet encapsulation (Column 6 Line 61-62); and a forwarding card (Figure 4) having an IP address table 90, the forwarding card to receive the number of IP packets from

the number of I/O cards and to forward the IP packets based on the IP address stored in the IP packet and the IP address table (Column 12 Line 6-15). Rao, however, does not disclose concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets. Ortega teaches concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets (step 5A and 5B in Figure 7). It would have been obvious to one skilled in the art to modify Rao to receive IP over Ethernet packets and Point-to-Point over Ethernet packets concurrently as taught by Ortega in order to support various networking protocols (Column 7 Line 2-4).

Regarding claim 16, Rao teaches a control card 26 having a database of configuration information, the configuration information used to configure the forwarding card and the number of I/O cards (Column 7 Line 3-16).

Regarding claim 33, Rao teaches a system comprising: a physical transmission line (Column 5 Line 8-10); and a network element 10, 14 coupled to the physical transmission line configured to, receive a number of Internet Protocol (IP) packets on a real circuit and a number of virtual circuits, wherein the real circuit is within the physical transmission line, the number of virtual circuits are within the real circuit such that the number of Internet Protocol (IP) packets on the real circuit have an IP over Ethernet encapsulation and the number of Internet

Protocol (IP) packets on the number of virtual circuits have a Point-to-Point over Ethernet encapsulation (Column 24 Line 30-39); deencapsulate the number of Internet Protocol (IP) packets having the IP over Ethernet encapsulation (Column 6 Line 61-62); deencapsulate the number of Internet Protocol (IP) packets having the Point-to-Point over Ethernet encapsulation (Column 6 Line 61-62); and forwarding the each of the deencapsulated Internet Protocol (IP) packets based on an IP address stored in it (Column 12 Line 6-15). Rao, however, does not disclose concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets. Ortega teaches concurrently receiving IP over Ethernet packets and Point-to-Point over Ethernet packets (step 5A and 5B in Figure 7). It would have been obvious to one skilled in the art to modify Rao to receive IP over Ethernet packets and Point-to-Point over Ethernet packets concurrently as taught by Ortega in order to support various networking protocols (Column 7 Line 2-4).

Regarding claim 34, Rao teaches the physical transmission line is one of a plurality of digital subscriber lines (DSL) coupled to the network element (Column 24 Line 52-54).

Response to Arguments

3. Applicant's arguments with respect to claim 1, 5-19 and 23-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the invention in general.

U.S. Patent 6,973,097 to Donzis et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2668

STEVEN NGUYEN
PRIMARY EXAMINER